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EXAMINER	
KANG, INSUN	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,636	KOCOT, REBECCA A.	
	Examiner	Art Unit	
	Insun Kang	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responding to the amendment filed on 9/27/2007.

2. Claims 1-20 are pending in the application.

Claim Objections

3. Claim 1-15 and 17 are objected to because of the following informalities: Per claims 1 and 8, "that" needs to be inserted into "to denote the designated instruction will proceed" and "to denote the non-designated instruction will not proceed" and per claim 17, "to denote the instruction addresses being designated will proceed." Per claim 6 and 14, "supserscalar" needs to be changed to superscalar. As per claims 2-5, 7-13, and 15, these claims are objected for dependency on the above objected parent claims 1 and 8. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Per claim 1:

It is unclear what "for display upon a screen that is accessible to a user" in line 2 means.

Interpretation: for display upon a screen is accessible to a user.

In line 1, the term "adapted for" is unclear. It has been held that the recitation that an element is "adapted for" perform a function is not a positive limitation but only requires the

ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. Correction is required.

Claim 1 recites the limitation "the sequence of instructions" in line 9 and "the instructions" in line 16, "the designated instruction" in line 12, and "the non-designated instruction" in line 17. There is insufficient antecedent basis for these limitations in the claim. In lines 17-18, "a succeeding stage" and "a user" in line 9 are interpreted as "the succeeding stage" and "the user."

Per claim 7:

It is unclear to which designator in line 7 it is referring. Interpretation: the designator. In line 10, "for all of the sequence of instructions" is interpreted as "for all instruction addresses of the sequence of instruction addresses." Claim 7 recites the limitation "the pipeline sequence" in line 11. There is insufficient antecedent basis for this limitation in the claim. Interpretation: the processor pipeline.

Per claim 8:

There is insufficient antecedent basis for the limitation, "the first instruction addresses" in line 16 in the claim. Interpretation: the first sequence of instruction addresses. It is unclear to what "processor" in lines 24, 29 (page 19) and 16(page 20) it is referring. Interpretation: "microprocessor." In line 29 (page 19), "the particular page" is interpreted as "the particular page of the microprocessor pipeline." Claim 8 recites the limitation "the sequence of instruction address" in line 27 (page 19), "the designated instruction" in line 2 (page 20), and "the first sequence of instructions" in line 16 (page 20). There is insufficient antecedent basis for these limitations in the claim.

Per claims 9 and 10:

The limitation, "instructions" is interpreted as "instruction addresses."

Per claim 12:

The limitation, "instruction" is interpreted as "instruction address."

Claim 14 recites the limitation "the pipeline" in 10. There is insufficient antecedent basis for this limitation in the claim. Interpretation: the microprocessor pipeline.

Per claim 15:

The limitations, "a pointing device," "a designator," "the stage name for all the sequence of instructions that will proceed to the next stage in the pipeline sequence" are unclear in meaning and interpreted as: the pointing device; the designator; a stage name for all instruction addresses of the first sequence of instruction addresses that will proceed to the succeeding stage in the microprocessor pipeline.

Claim 16 recites the limitation "the pipeline." There is insufficient antecedent basis for this limitation in the claim. Interpretation: the processor pipeline.

Claim 17 recites the limitation "the next stage of the pipeline" in the last line. There is insufficient antecedent basis for this limitation in the claim. Interpretation: the succeeding stage of the processor pipeline.

As per claims 2-6, 11, 13, and 18-20, these claims are rejected for dependency on the above rejected parent claims.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions

and requirements of this title.

7. Claims 1-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-15 are non-statutory because they are directed to a computer program per se that does not fit within the definition of the categories of patentable subject matter set forth in § 101. Therefore, the claims are non-statutory. Recommendation: Per claim 1, "A graphics rendering engine stored on a computer-storage medium and executable by a computer." per claim 8, "A software development tool stored on a computer-storage medium and executable by a computer."

The following link on the World Wide Web is for the United States Patent And Trademark Office (USPTO) policy on 35 U.S.C. §101. The following link on the World Wide Web is for the United States Patent And Trademark Office (USPTO) policy on 35 U.S.C. §101. <http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf>

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 2, and 4-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Aihara (US PG Pub. 2003/0110476).

Per claim 1:

Aihara discloses:

-a sequence of instruction addresses adapted for display upon a screen that is accessible to a user (i.e. page 5, 0062; 0073);

-a sequence of processor pipeline stages attributable to respective ones of the sequence of instructions and, during times when a user selects one of the instruction addresses (i.e. page 3, 0046);

- the screen displays: a designator for at least one of the instructions to denote the designated instruction will proceed to a succeeding stage in the processor pipeline during a next clock cycle; and a non-designator for another one of at least one of the instructions to denote the non-designated instruction will not proceed to a succeeding stage in the processor pipeline during the next clock cycle (i.e. page 5, 0062; 0064; 0074).

Per claim 2:

Aihara further discloses:

- the screen comprises a graphical user interface (GUI) (i.e. page 5, 0062; 0073).

Per claim 4:

Aihara teaches that the designator is a color that highlights the stage attributable to the at least one instruction that will proceed to the succeeding stage (i.e. page 5 lines 0064).

Per claim 5:

Martinez further discloses:

- wherein the color differs depending on which stage is highlighted (i.e. page 5 lines 0064).

Per claim 6:

Aihara further discloses:

- wherein the processor pipeline is a pipeline of a superscalar processor where more than one instruction can exist within each stage of the pipeline (i.e. page 1, 0005;page 4, 0055).

Per claim 7:

Aihara further discloses:

- wherein the user actuates a pointing device to select only one of the instruction addresses and, in response thereto, the window displays a designator over a stage number field bearing the stage name for all of the first sequence of instructions that will proceed to the next stage in the pipeline sequence (i.e. page 5, 0064).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 8-10 and 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aihara (US PG Pub. 2003/0110476) in view of Beatty et al. (US Patent 5,913,052) hereafter

Beatty.

Per claim 8:

Aihara discloses a graphics data processing system (i.e. page 5, 0062; 0073); source code represented as a first sequence of instruction addresses (i.e. page 5, 0062); a graphics rendering engine coupled to receive the first instruction addresses and produce a graphical user interface (GUI) window (i.e. Fig. 11, the display device for the displaying module 15).

Aihara does not explicitly teach that the graphical user interface debugger includes a breakpoint field upon receiving user input via a pointing device selects a particular instruction address within the first sequence of instruction addresses shown in a particular stage of a processor pipeline. However, Beatty teaches using a breakpoint circuitry was known in the pertinent art, at the time applicant's invention was made, to allow a user to "establish at least one breakpoint for interrupting the operation of" a program (i.e. col. 3 lines 52-57). It would have been obvious for one having ordinary skill in the art to modify Aihara's disclosed debugger to incorporate the teachings of Beatty. The modification would be obvious because one having ordinary skill in the art would be motivated to "predefine pausing points, permitting the user to examine DSP states at the breakpoints (i.e. col. 3 lines 52-57)."

Aihara further discloses: displays all instruction addresses within the first sequence of instruction address along with corresponding stages of the processor pipeline during a clock cycle in which the particular instruction address is within the particular stage (i.e. page 3, 0046); assigns a designator to at least one instruction address of the first sequence of instruction addresses to denote the designated instruction will proceed to a succeeding stage in the

microprocessor pipeline during a clock cycle succeeding the clock cycle (i.e. page 5, 0062; page 6, 0076); assigns a non-designator to denote a non-designated instruction within the microprocessor pipeline (i.e. page 5, 0062; 0064; 0074); an instruction address field that, upon selection by a user via the pointing device, allows the user to move said another at least one instruction address (i.e. page 6, 0080);

a scheduler that responds to the moved said another at least one instruction address to form a second sequence of instructions that has a higher instruction throughput in the processor pipeline than the first sequence of instructions (i.e. page 5, 0063).

Per claim 9:

Aihara further discloses:

- wherein the graphics rendering engine further displays all instructions within the first sequence of instructions and assigns a designator to a number of the instruction address of the second sequence of instructions that exceed a number of the at least one instruction address of the first sequence of instruction addresses (i.e. page 5, 0062).

Per claim 10:

Aihara further discloses:

-wherein the second sequence of instructions requires fewer clock cycles through the processor pipeline than the first sequence of instructions (i.e. page 4, 0057).

Per claims 12-15, they are the method versions of claims 4-7, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 4-7 above.

Per claim 16:

Aihara discloses a debugger system displaying progression of instruction addresses through a processor pipeline (i.e. page 5, 0062; 0073). Aihara does not explicitly teach that the graphical user interface debugger includes a breakpoint field that allows a user to select a breakpoint within a breakpoint column of a display screen to select an instruction address within the same line as the breakpoint. However, Beatty teaches using a breakpoint circuitry was known in the pertinent art, at the time applicant's invention was made, to allow a user to "establish at least one breakpoint for interrupting the operation of" a program (i.e. col. 3 lines 52-57). It would have been obvious for one having ordinary skill in the art to modify Aihara's disclosed debugger to incorporate the teachings of Beatty. The modification would be obvious because one having ordinary skill in the art would be motivated to "predefine pausing points, permitting the user to examine DSP states at the breakpoints (i.e. col. 3 lines 52-57)."

Aihara in view of Beatty further discloses:

-a clock cycle associated with the selected instruction address being in a stage within the processor pipeline (i.e. page 3, 0046); designating all instruction addresses within the processor pipeline that will proceed to the succeeding stage of the pipeline; and not designating all instruction addresses within the processor pipeline that will not proceed to the succeeding stage of the pipeline (i.e. page 5, 0062; 0064; 0074).

Per claim 17:

Aihara further discloses:

- wherein said designating comprises receiving a signal from a stage debug register by a graphics rendering engine to denote the instruction addresses being designated will proceed to the next stage of the pipeline (i.e. page 5, 0074).

Per claim 18:

Aihara further discloses:

- wherein said designating comprises checking resources of a processor to determine if the instruction addresses will be allowed to proceed and, if so, sending a signal from a debug register that stores the checking outcome to designate the instruction addresses that have corresponding resources available to allow such instruction addresses to proceed (i.e. page 5, 0074).

Per claims 19 and 20, they are the method versions of claims 12 and 13, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 12 and 13 above.

12. Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aihara (US PG Pub. 2003/0110476) in view of Beatty et al. (US Patent 5,913,052) hereafter Beatty, and further in view of Hill et al. (Pg. Pub. 2002/0130871) hereafter Hill.

Per claim 11:

Aihara and Beatty do not explicitly teach that the window comprises a pop-up window rendered upon a computer display screen. However, Hill teaches such a pop-up window was

known in the pertinent art, at the time applicant's invention was made, to display additional information without using a standard window (i.e. 0102). It would have been obvious for one having ordinary skill in the art to modify the system of Aihara and Beatty to incorporate the teachings of Hill. The modification would be obvious because one having ordinary skill in the art would be motivated to display a pop-up window for additional information if desired.

Per claim 3, it is the engine version of claim 11, respectively, and is rejected for the same reasons set forth in connection with the rejection of claim 11 above.

Response to Arguments

13. Applicant's arguments, filed on 9/27/2007, with respect to the rejection(s) of claim(s) 1-20 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Aihara and Beatty. Therefore, this action is made non-final.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Insun Kang whose telephone number is 571-272-3724. The examiner can normally be reached on M-R 6:30-5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MENG AI AN can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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